Customer No.: 31561
Application No.: 10/604,692
Docket No.: 10156-US-PA

AMENDMENTS

In the Claims:

1. (currently amended) A split-gate non-volatile memory cell, comprising:

a substrate;

a charge-trapping layer on the substrate;

a split gate on the charge-trapping layer, including ~~at least one split region directly over the charge-trapping layer~~ two or more separate conductive pieces shorted with each other, wherein ~~the split gate comprises at least~~ any two ~~separated~~ neighboring conductive pieces ~~that are shorted with each other and are arranged adjacently to form the at least one split region without any other conductor in the at least one split region~~ have two opposite edge portions over the charge-trapping layer that together cause, in operation of the memory cell, a locally stronger electric field such that only one coding region is defined, by the two neighboring conductive pieces, in the charge-trapping layer around the two opposite edge portions; and

a source/drain in the substrate beside the split gate~~, wherein~~

~~the charge-trapping layer around the split region serves as a coding region~~.

Claims 2-3. (canceled)

4. (previously presented) The split-gate non-volatile memory cell of claim 1, wherein the conductive pieces of the split gate include a pair of conductive spacers and a conductive layer between the pair of conductive spacers.

5. (original) The split-gate non-volatile memory cell of claim 4, wherein the pair of conductive spacers are arranged with two substantially vertical sidewalls thereof adjacent to the source/drain.

6. (original) The split-gate non-volatile memory cell of claim 5, further comprising an insulator on the source/drain, wherein the pair of conductive spacers are disposed on the sidewalls of the insulator.

Claim 7. (canceled)

8. (previously presented) The split-gate non-volatile memory cell of claim 1, wherein the conductive pieces are separated from each other by a dielectric layer.

9. (original) The split-gate non-volatile memory cell of claim 1, wherein the split gate comprises polysilicon.

10. (original) The split-gate non-volatile memory cell of claim 1, wherein the charge-trapping layer comprises a silicon nitride layer disposed between two silicon oxide layers.

11. (original) The split-gate non-volatile memory cell of claim 1, wherein the charge-trapping layer comprises aluminum oxide (Al_2O_3).

12. (original) The split-gate non-volatile memory cell of claim 1, wherein the substrate comprises a p-substrate, and the source/drain comprises an n-type source/drain.

Claims 13-34. (canceled)

35. (currently amended) An operating method of a split-gate non-volatile memory cell, wherein

the split-gate non-volatile memory cell comprises:

a substrate;

a charge-trapping layer on the substrate;

a split gate on the charge-trapping layer, including ~~at least one split region directly over the charge-trapping layer~~ two or more separate conductive pieces shorted with each

other, wherein ~~the charge-trapping layer around the split region serves as a coding region, the split-gate comprises at least~~ any two ~~separated~~ neighboring conductive pieces ~~that are shorted with each other and are arranged adjacently to form the at least one split region without any other conductor in the at least one split region~~ have two opposite edge portions over the charge-trapping layer that together cause, in operation of the memory cell, a locally stronger electric field such that only one coding region is defined, by the two neighboring conductive pieces, in the charge-trapping layer around the two opposite edge portions; and

a source/drain in the substrate beside the split gate, and

the operating method comprises:

in a programming operation:

applying 0V to the substrate and the source/drain; and

applying a first negative voltage to the split gate, the first negative voltage being sufficiently high for injecting electrons into the coding region; and

in an erasing operation:

applying 0V to the split gate, wherein each conductive piece is at an electric state of 0 V;

floating the source/drain; and

applying a second negative voltage to the substrate, the second positive voltage being sufficiently high for ejecting electrons from the coding region.

36. (original) The operating method of claim 35, wherein the first negative voltage is about –10V.

37. (original) The operating method of claim 35, wherein the second negative

voltage is about –10V.

Claims 38-45: (canceled).